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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RADOSEVICH, STEVEN D	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,097	JARABEK ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *9,10,19,20,27 and 28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-18 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *20 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-8, 11-18, and 21-26 are present in this Response to applicants instant Response. Acknowledgement is made that claims 9, 10, 19, 20, 27, and 28 have been cancelled and are not presented in this examination.

Drawings

The drawings (figures 1 and 4) previously objected to have been amended and are accepted. The examiner does not see any other informalities or errors within the drawings at this time that would result in the drawings being further objected.

Response to Arguments

Applicant's arguments with respect to claim 1-8, 11-18, and 21-26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Lemone (US Patent 4171765) and further in view of Loaiza et al. (US patent 6928607 B2).

1. As per claims 1 and 13 Lemone teaches:

Generating a first check word based on incoming data ("write" error word, line 29-30);

Generating a second check word based on stored data ("read" error word, line 33);

Comparing the first check word to the second check word (lines 36-39);

Generating a comparison result (remainder); and

Indicating a failure (non-zero, line 43) based on the comparison result (column 1 lines 15-60).

Lemone does not specifically teach:

Storing the first check word in a write accumulator;

Storing the second check word in a read accumulator; and

Comparing the first check word and the second check word by way of a compare circuit connected to the write accumulator and the read accumulator.

However in an analogous art Loaiza teaches wherein the first and second check words are not stored within the nonvolatile memory with the data and are compared to each other to verify that the data has not been corrupted.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to incorporate the teaches of Loaiza wherein the first and

second check words are stored within a write and read accumulator or buffers that requires no overhead space within the memory and are compared to each other to verify data not been corrupted into the teaches of Lemone so as to reduce the "overhead" and required memory to store the data being checked for corruption/errors as indicated by Loaiza (column 1 lines 29-45, columns 2-3, and claims 6-7).

2. As per claims 2 and 14, Lemone teaches the above as per claim 1 and 13, wherein generating the second check word occurs at a time subsequent to the data being stored and prior to the data being overwritten (column 1 lines 29-32).

3. As per claims 3 and 15, Lemone teaches the above as per claims 1 and 13, further comprising: generating the second check word during periods of time when the device storing the data is in an idle state (column 1 lines 29-36).

4. As per claims 4 and 16, Lemone teaches the above as per claims 1 and 13, further comprising: synchronizing the generation of the second check word to the reading and writing of the data (column 1 lines 29-36).

5. As per claims 5 and 17, Lemone teaches the above as per claims 1 and 13, wherein generating the second check word further comprises reading bytes from a selected set of memory locations (column 1 lines 35-36).

6. As per claim 6, Lemone teaches the method above as per claims 5 and 17, wherein the selected set of memory locations includes memory locations included in a single memory (column 1 line 16 and figures 1, 3, 4, and 5).

7. As per claim 18, Lemone teaches the above as per claims 1 and 13, wherein the second check word is generated by multiple data words read simultaneously from a memory (column 1 line 35-36).

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lemone as modified with Loaiza as applied to claim 6 above, and further in view of Katayama et al. (US 6388920 B2).

8. As per claim 7, Lemone teaches the method above as per claim 6.

Lemone does not specifically teach the method wherein the selected set of memory locations includes memory locations included in multiple memories.

However, in an analogous art Katayama teaches reading selected set of memory locations includes memory locations included in multiple memories (52 – figure 6 and column 16 lines 38-41).

Therefore, one would be motivated to combine the above teachings of Lemone and Katayama in-order to reduce processing time by accessing multiple memories simultaneously.

9. As per claim 8, Katayama teaches reading the multiple memories simultaneously (column 16 line 41).

Claims 11-12 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lemone (US patent 4171765), in view of Loaiza et al. (US patent 6928607 B2), and further in view of Katayama et al. (US 6388920 B2).

10. As per claim 11, Lemone teaches generating a first check word based on incoming data ("write" error word, line 29-30); reading a set of data stored in memory

(column 1 lines 35-36); generating a second check word based on the set of data ("read" error word, line 33); comparing the first check word to the second check word (lines 36-39); generating a comparison result (remainder); and indicating a failure (non-zero, line 43) based on the comparison result (column 1 lines 15-60).

Lemone does not specifically teach generating a first check word based on incoming data to a subset of a plurality of memories or reading a set of data stored in the subset of the memories.

However, in an analogous art Katayama teaches generating a first check word (66 - figure 7 and column 16 line 1) based on incoming data (write data – column 15 line 48) to a subset (53 and 54 – figure 6) of a plurality of memories (52 – figure 6) and reading a set of data stored in the subset (53 and 54 - figure 6) of the memories (column 16 lines 22-23).

Therefore, one would be motivated to combine the above teachings of Lemone and Katayama in-order to reduce processing time by accessing multiple memories and in determining whether an error is present in data words which are being read from a data storage element as indicated by Lemone (column 1 lines 11-13).

Lemone as modified with Katayama does not specifically teach:

Storing the first check word in a write accumulator;

Storing the second check word in a read accumulator; and

Comparing the first check word and the second check word by way of a compare circuit connected to the write accumulator and the read accumulator.

However in an analogous art Loaiza teaches wherein the first and second check words are not stored within the nonvolatile memory with the data and are compared to each other to verify that the data has not been corrupted.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to incorporate the teaches of Loaiza wherein the first and second check words are stored within a write and read accumulator or buffers that requires no overhead space within the memory and are compared to each other to verify data not been corrupted into the teaches of Lemone as modified with Katayama so as to reduce the "overhead" and required memory to store the data being checked for corruption/errors as indicated by Loaiza (column 1 lines 29-45, columns 2-3, and claims 6-7).

11. As per claim 12, Katayama teaches reading a set of data stored in the predetermined subset of the memories includes reading data from multiple memories simultaneously (column 16 lines 38-41 and figure 6).

12. As per claim 21, Lemone teaches generating a first check word based on incoming data ("write" error word, line 29-30); reading a set of data stored in memory (column 1 lines 35-36); generating a second check word based on the set of data ("read" error word, line 33); comparing the first check word to the second check word (lines 36-39); generating a comparison result (remainder); and indicating a failure (non-zero, line 43) based on the comparison result (column 1 lines 15-60).

Lemone does not specifically teach storing data in multiple memories, generating a first check word based on incoming data to a predetermined subset of the memories, and reading a set of data stored in the predetermined subset of the memories.

However, in an analogous art Katayama teaches storing data in multiple memories (52 – figure 6), generating a first check word based on incoming data to a predetermined subset of the memories (column 16 line 1 and figure 7), and reading a set of data stored in the predetermined subset of the memories (54 – figure 6 and 52 – figure 6).

Therefore, one would be motivated to combine the above teachings of Lemone and Katayama in-order to reduce processing time by accessing multiple memories and in determining whether an error is present in data words which are being read from a data storage element as indicated by Lemone (column 1 lines 11-13).

Lemone as modified with Katayama does not specifically teach:

Storing the first check word in a write accumulator;

Storing the second check word in a read accumulator; and

Comparing the first check word and the second check word by way of a compare circuit connected to the write accumulator and the read accumulator.

However in an analogous art Loaiza teaches wherein the first and second check words are not stored within the nonvolatile memory with the data and are compared to each other to verify that the data has not been corrupted.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to incorporate the teaches of Loaiza wherein the first and

second check words are stored within a write and read accumulator or buffers that requires no overhead space within the memory and are compared to each other to verify data not been corrupted into the teaches of Lemone as modified with Katayama so as to reduce the "overhead" and required memory to store the data being checked for corruption/errors as indicated by Loaiza (column 1 lines 29-45, columns 2-3, and claims 6-7).

13. As per claim 22, Lemone teaches generating the second check word at a time subsequent to the data being stored and prior to the data being overwritten (column 1 lines 29-32).

14. As per claim 23, Lemone teaches generating the second check word during periods of time when the device storing the data is in an idle state (column 1 lines 29-36).

15. As per claim 24, Lemone teaches synchronizing the generation of the second check word to the reading and writing of the data (column 1 lines 29-36).

16. As per claim 25, Lemone teaches generating the second check word by reading bytes from a selected set of memory locations (column 1 lines 35-36).

17. As per claim 26, Lemone teaches the second check word is generated by multiple data words read simultaneously from a memory (column 1 line 35-36).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2138

GUY LAMARRE
PRIMARY EXAMINER